***Smart-Home Controller using a Basys3 FPGA Development Board***

FPGA Project Group: [Your group number]

[1st Member Name], [1st Member Uni ID]

[2nd Member Name], [2nd Member Uni ID]

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ANU College of Engineering, Computing and Cybernetics

The Australian National University

Table of Contents

[1 INTRODUCTION 3](#_Toc131608758)

[2 RESOURCE REQUIREMENTS 3](#_Toc131608759)

[3 DESIGN METHODOLOGY 3](#_Toc131608760)

[3.1 Function I: Secure Garage Door Control 3](#_Toc131608761)

[3.1.1 Assumptions 3](#_Toc131608762)

[3.1.2 Inputs and Outputs 3](#_Toc131608763)

[3.1.3 FSM Design 4](#_Toc131608764)

[3.1.4 Module Hierarchy 4](#_Toc131608765)

[3.1.5 Implementation 4](#_Toc131608766)

[3.2 Function II: Climate Control (Home Heating and Cooling) 4](#_Toc131608767)

[3.3 Integrated Design: Smart-home Controller 4](#_Toc131608768)

[3.3.1 Module Hierarchy 4](#_Toc131608769)

[3.3.2 User Interface 4](#_Toc131608770)

[4 DESIGN CONSIDERATIONS 4](#_Toc131608771)

[5 RESULTS & DISCUSSION 4](#_Toc131608772)

[References 5](#_Toc131608773)

[Appendix I: Verilog Code 6](#_Toc131608774)

[Appendix II: [Appendix Title] 7](#_Toc131608775)

# INTRODUCTION

Provide background information on the project, including its purpose, scope, and objectives. Include an outline of the whole report.

Use the following formatting guidelines for this report:

* Font: Times New Roman
* Font size:
  + 12pt for the body text
  + 14pt for Level-3 Headings
  + 16pt for Level-2 Headings
  + 20pt for Level-1 Heading
  + 10pt for captions of table and figures
* Use 1.15 line spacing for the body text.
* Page margin: Moderate
* Use the given header and footer.
  + Update your course code on the header
  + Update your group number on the footer
* Use different heading levels to structure your report.
* Content must not exceed 10 pages and any content beyond this page limit will not be assessed. Note that title page, table of contents, references, and appendices do not count toward this page limit.

# RESOURCE REQUIREMENTS

What resources are required to implement this project?

# DESIGN METHODOLOGY

The following section breakdown is suggested in this section, but you are free to adapt the template as you see fit.

## Function I: Secure Garage Door Control

Describe the intended function with desired features and clearly state any additional features if implemented.

### Assumptions

Include the assumptions you made before designing this function.

### Inputs and Outputs

Describe the inputs/outputs of this function, e.g., SW[0]: GARAGE\_CONTROL, LD4 to LD0: Door status

### FSM Design

Explain how you designed the FSM using state-diagrams and/or tables. Describe each state, next-state transitions, and outputs.

### Module Hierarchy

Explain the module hierarchy using block diagrams at the sub-module level with interconnections between the inputs and outputs.

Explain each sub-module. You can make each sub-module a different section under this heading.

### Implementation

Using the module structure, explain the operation and implementation. How do the inner workings of your design allow it to behave as required? Was any part of the design verified using simulations?

## Function II: Climate Control (Home Heating and Cooling)

Follow a similar structure to Function I. Add or remove sub-headings as appropriate.

## Integrated Design: Smart-home Controller

Explain the integrated design of two functions.

### Module Hierarchy

Explain the module hierarchy using block diagrams with interconnections of inputs and outputs between sub-modules. If you have given a detailed diagram on Function I and II in the sections before, this section need to include only how the highest-level modules and external I/Os are connected.

### User Interface

Include a picture of Basys3 board with markings of your inputs and outputs. Particularly explain inputs/outputs exclusive to the integrated design.

# DESIGN CONSIDERATIONS

What were your design considerations: choice of clock frequencies, use of debouncers, how you dealt with asynchronous inputs [1], reset/initialization conditions [2], etc. Justify these considerations. Any techniques used to optimize your design?

# RESULTS & DISCUSSION

How did the design perform? What are the strength and weaknesses of your design? Discuss the challenges faced during the design process and how you overcame them. How can the design be improved further? Scope for future developments? What were your main learning outcomes?

# References

List of sources cited in the report

1. J. Wakerly, *Digital Design: Principles and Practices*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1994.
2. S. Kilts, *Advanced FPGA Design: Architecture, Implementation, and Optimization*. Hoboken, NJ, USA: Wiley, 2007.

# Appendix I: Verilog Code

|  |
| --- |
| always @(posedge clk) begin  if (reset) begin  accumulator = 32’d0;  end else begin  accumulator = accumulator + increment;  end  end |

# Appendix II: [Appendix Title]

In appendixes, you can include any simulation results, big diagrams or tables, pictures of results, etc.